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Study of Geometrical structure of Perfect Difference Network (PDN)

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Abstract: Geometrical Structure of PDN architecture can be considered as a parameter for critical study for connectivity and complexity of interconnection network. This paper illustrates the new pattern and properties for improving performance and latency time and is also useful for path selection, fast and secure communication system between processors. In this paper the mapping and message passing problem/method is also discussed, which allows the use of standard tools for solving it/problems. Mapping between processor is done for a study of geometrical structure between processor. The main objective of this paper is to simplify the design and increase the performance of Perfect Difference Network. Out of which we have obtained several pattern and property which is mention in this paper.

Keywords: Perfect Difference Network, Interconnection Networks, Pattern, message passing, Topological properties, modelling, Bit Manipulation.

I. INTRODUCTION

In this paper we have studied to explore Interconnection Network to enhance the performance of Perfect Difference Network. Research in Interconnection Network is a broad field, where most results have been achieved for a multitude of Perfect Difference Network (PDN) particularly in parallel and distributed system. A large number of models, algorithms, structure and lemmas have been proposed in the last few years for Perfect Difference Network (PDN).

Perfect difference sets were discussed in 1938 by J.Singer [1] The formulation was in terms of points and lines in a finite projective plane. The perfect difference sets considered for being developed into a interconnect network mainly through works of Behrooz Parhami and Mikhail A Rakov [2]. In their, perfect difference network (PDN) interconnection, they have shown that PDN interconnection scheme is optimal in the sense that it can accommodate an asymptotically maximal number of nodes with smallest possible node degree under the constraint of the network diameter being two.They have compared PDNs and some of their derivatives to interconnection networks with similar cost and performance, including certain generalized hypercube and their hierarchical variants.

Topological properties [3] of perfect difference network compared with the corresponding properties of hypercube. In this scheme, sparse linear system was implemented. It was proved that access function or routing function to map data on hypercube contains topological properties. [3]

Perfect difference networks are a robust high-performance interconnection network for parallel and distributed systems. A comparative study of hypercube and perfect difference network was done, based on topological properties.[4]

An open source NS2 simulator used by Priyanka Wankar et. all [5] to measure the performance analysis and implementation of PDN. Formula $n=\delta^2+\delta+1$ is tested on simulator. It was found that simulated PDN and the Mathematical underpinnings makes, it desirable as robust and high-performance.

II. METHODOLOGY

Diameter can be considered as an important parameter for study of the structural relationship [6] and complexity (time and cost) of interconnection network. Diameter is inversely proportional to the cost of interconnection network but directly proportional to time and meanwhile it affects the communication of interconnection network.

Mapping illustrates how to assign task to a processor of PDN such that it maximize utilization of system resources while minimizing the latency time/communication time. An important point to take into consideration is that the execution of multiple instruction/data on the same processor is not allowed, as this provides a fall of performance in this type of architecture.

III.RESULT AND DISCUSSION

This section helps to take mapping decision [7] at statically or dynamically by different methods for Perfect Difference Network. Topological Properties are used to map the relationship [7] [8] between processor for Perfect Difference Network. Communication links are bidirectional; it is used for both read and executes program instructions

- MAPPING AND TRANSFORMATION BETWEEN PROCESSOR OF PERFECT DIFFERENCE NETWORK

In reference of definition of Perfect Difference Network [9] there are $\delta 2$ $+\delta+1$ node/core/processor. Message

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passing mechanism [10] between processors of perfect difference network is illustrated below:

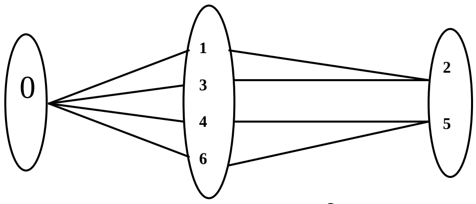

Fig 1: Relationship of p_0 with $\delta^2 + \delta$ processors

Processor p_0 has the capability to broadcast same instruction for p_1, p_3, p_4, and p_6 simultaneously. p_0 may used P_1 or p_3 to communicate with p_2 and p_4 or p_6 are used to communicate with p_5.

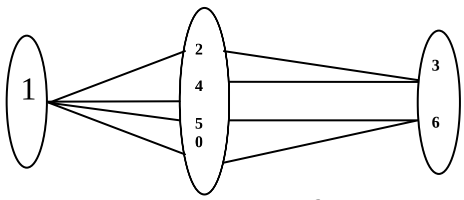

Fig 2: Relationship of p_1 with $\delta^2 + \delta$ processors

Processor p_1 has the capability to broadcast same instruction for p_2, p_4, p_5, and p_0 simultaneously. P_1 may used P_2 or p_4 to communicate with p_3 and p_5 or p_0 are used to communicate with p_6.

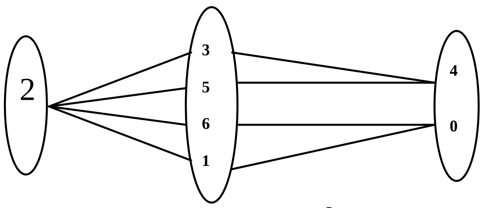

Fig 3: Relationship of p_2 with $\delta^2 + \delta$ processors

Processor p_2 has the capability to broadcast same instruction for p_3, p_5, p_6, and p_1 simultaneously. P_2 may used P_3 or p_5 to communicate with p_4 and p_6 or p_1 are used to communicate with p_0.

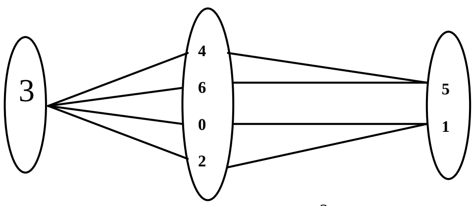

Fig 4: Relationship of p_3 with $\delta^2 + \delta$ processors

Processor p_3 has the capability to broadcast same instruction for p_4, p_6, p_0, and p_2 simultaneously. P_3 may used P_4 or p_6 to communicate with p_5 and p_0 or p_2 are used to communicate with p_1.

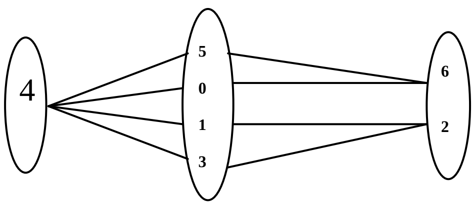

Fig 5: Relationship of p_4 with $\delta^2 + \delta$ processors

Processor p_4 has the capability to broadcast same instruction for p_5, p_0, p_1, and p_3 simultaneously. P_4 may used P_5 or p_0 to communicate with p_6 and p_1 or p_3 are used to communicate with p_2.

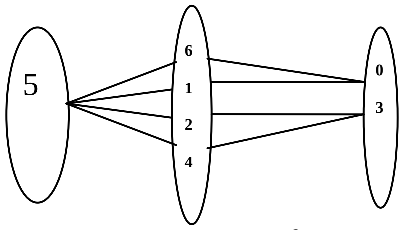

Fig 6: Relationship of p_5 with $\delta^2 + \delta$ processors

Processor p_5 has the capability to broadcast same instruction for p_6, p_1, p_2, and p_4 simultaneously. P_5 may used P_6 or p_1 to communicate with p_0 and p_2 or p_4 are used to communicate with p_3.

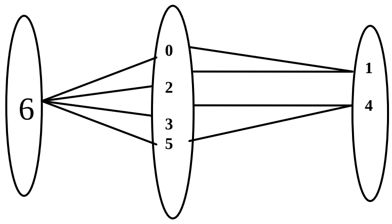

Fig 7: Relationship of p_6 with $\delta^2 + \delta$ processors

Processor p_6 has the capability to broadcast same instruction for p_0, p_2, p_3, and p_5 simultaneously. P_6 may used P_0 or p_2 to communicate with p_1 and p_3 or p_5 are used to communicate with p_4.

These analysis/study are an abstraction of a message passing model to communicate among processors of Perfect Difference Network.

In this analysis it can be concluded that the pi has several transitive relations, which are given in the table1.

Table 1: Transitive relation of p_i

Node/processor/ core[p_i]	**Node having transitive relation**
0	2,5
1	3,6
2	4,0
3	5,1
4	6,2
5	0,3
6	1,4

Table 2: PDS relationship between pi and $pi_{transitive}$.

PDS(p_i)	PDS($pi_{transitive}$)
(0-0)	(3-1) , (1-3)
(1-0)	(3-0) , (0-1)
(3-1)	(0-3) , (0-0)
(3-0)	(1-3) , (1-0)
(0-3)	(0-1) , (3-1)
(1-3)	(0-0) , (3-0)
(0-1)	(1-0) , (0-3)

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Algorithm 1: **MACBPPDN**

BEGIN

STEP 1: Declare all the variable

STEP 2: Assign memory allocation to the PDS.

STEP 3: Input value of δ.

STEP 4: Validate the δ value

(i) Is value of δ is prime or power of prime.
(ii) The PDS value of particular delta (δ) is available or not.

STEP 5: Input Source (p_s) and Destination (p_d).

STEP 6: Evaluate the formula/ equation

// using structural relation study

STEP 7: Display the Result.

END

The main objective of this algorithm is to select paths of small total delay for each data/instruction. If there were no queuing delays along any link, the path selection would be simple. The time for a data/instruction to travel between two processors is O(2),assuming no queuing delays at the links.

• BOOLEAN OPERATION ON STATE OF PDN

While doing mapping several structure[11][12] and pattern have been find out. Bit representation/state of processors are useful for designing circuits [13]and it may model a logical system with a single equation. The three operation AND, OR,EOR(exclusive or) are used in the state of processors which is found by transitive table [7][14] of Perfect Difference Network. The main objective of this section is to simplify the design and increase the performance of Perfect Difference Network. Out of which we have obtained several pattern and property which is mention below.

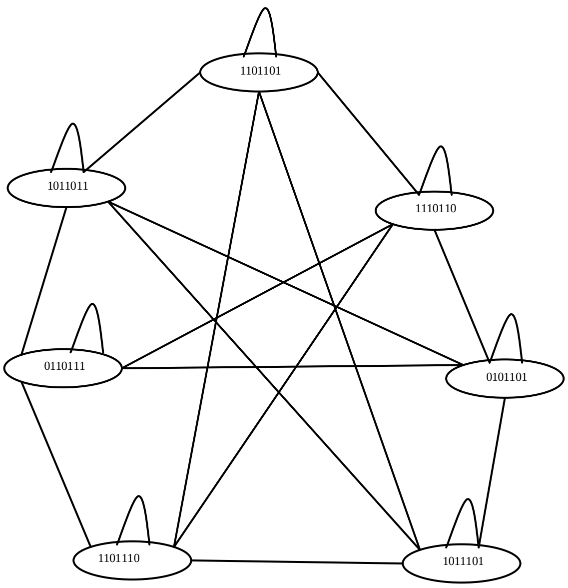

Fig 8:State Diagram

Table 3:AND operation on fstate(PDN(TT))

AND	**1**	**1**	**0**	**1**	**1**	**0**	**1**
1	1	1	0	1	1	0	1
1	1	1	0	1	1	0	1
0	0	0	0	0	0	0	0
1	1	1	0	1	1	0	1
1	1	1	0	1	1	0	1
0	0	0	0	0	0	0	0
1	1	1	0	1	1	0	1

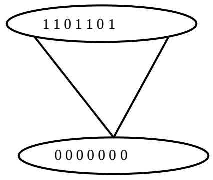

fig 9:relationship between state of table 3.

Fig. 9 shows the relationship between state of AND operation, there are two bits (0) is match (3^{rd} & 6^{th} position of state) counting starts from left to right.

Table 4:OR operation on fstate(PDN(TT))

OR	**1**	**1**	**0**	**1**	**1**	**0**	**1**
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1

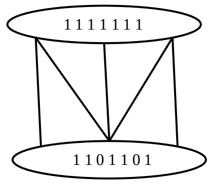

fig 10:relationship between state of table 4.

Fig.10 shows the relationship between state of OR operation, there are five bits (1) is match (0^{th}, 1, 3^{rd}, 4^{th}, & 6^{th} position of state) counting starts from left to right.

Table 5:X-OR operation on fstate(PDN(TT))

E-OR	**1**	**1**	**0**	**1**	**1**	**0**	**1**
1	0	0	1	0	0	1	0
1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	1
1	0	0	1	0	0	1	0
1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	1
1	0	0	1	0	0	1	0

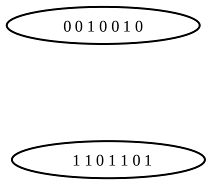

fig 11:relationship between state of table 5.

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Note: No node in PDN founds to be mutually exclusive which shows that PDN is well connected to each other hence proved that PDN is robust.

From the above studied it can be concluded that, if we apply the EOR operation between the state of OR, we get an indirect relation of processor p_i and if we apply the EOR operation between the state of AND, we get a direct relation of processor p_i.

- INTERCONNECTION WITH NODE X

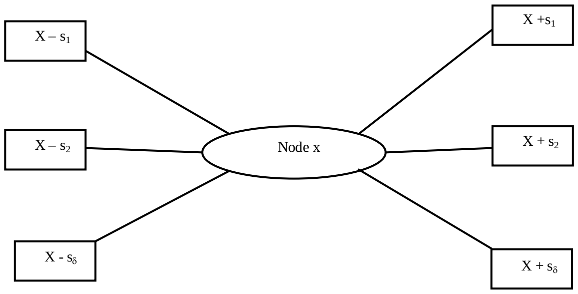

Fig.12: interconnection with p_x.

This section shows the direct interconnection network [15] with n=$\delta^2 + \delta + 1$ nodes based on the normal form perfect difference set { s0, s1, . . . , sδ } with order δ.

Node x is connected via directed links to nodes i±1 and i±sj(mod n), for $2 \leq j \leq \delta$ [2][3][6]. For each link from node x to others, the reverse link from others to node x is also possible. The communication between nodes in a PDN is Symmetric and from the above studied it can be already proved the communication between nodes in a PDN is also transitive [16][17][18].

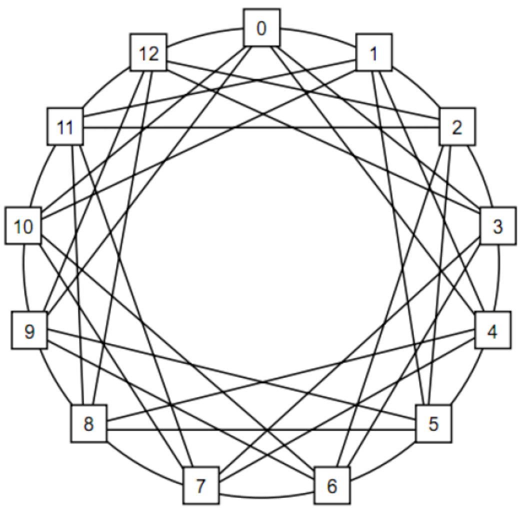

Fig 13: PDN with *n* = 13 nodes based on the perfect difference set {0, 1, 3, 9}.

IV. CONCLUSION

The focus of this paper is on modelling the mapping and message passing problem which allows the use of standard tools for solving it. Mapping between processor is done for a study of geometrical structure between processor.
PDN can be used for Network-on-Chip (NoC). NoC is a technique based on System-on-Chip (SoC) which attempts to provide high performance nanoscale architectures [18]. Network can be made reusable by separating the communication infrastructure from computing resources.

A perfect difference network is a robust, high performance interconnection network for parallel and distributed computation. PDNs may be desirable for large networks with wired connectivity, but definitely they do offer attractive alternatives for wireless, nanophotonic and optical interconnections and as smaller component networks in hierarchical architectures.

From the above observation/analysis it can be conclude that diameter should have a balanced value. There are ($\delta^2 + \delta + 1$) processors having transitive operation with each other and each nodes come in two times in transitive relation (as in table 1).

We have also observed that the pi has not always direct relation with its mirror image because the pi has direct relation with 2δ processors and transitive relation with others. The mirror image of pi can have its transitive relationship with pi. Relational study between node i and its connected node also has transitive relation using PDS

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REFERENCES

[1] Singer, J. "A theorem in Finite Projective Geometry and Some Applications to Number Theory". Trans American Mathematical Society, Vol.43,pp377-385,1938.

[2] Parhami, Behrooz and Rakaov, Mikhail."Perfect Difference Networks and Related Interconnection structures for Parallel and Distributed Systems". IEEE Journal on Parallel and Distributed Systems 16(8):725-736, 2005.

[3] Katare, R.K. and Chaudhari, N.S "Study of Topological Property of Interconnection Networks and its mapping to Sparse Matrix Model", International Journal of Computer Science and Applications,2009 Technomathematics Research Foundation.Vol. 6, No. 1, pp. 26 – 39.

[4] Katare, R.K and Chaudhari,N.S. "A Comparative study of hypercube and perfect difference network for parallel and distributed systems and its application to sparse linear system". Vladimir Journal of Computer Information Sciences, Vol2, Sandipani Academy, Ujjain(M.P.),India pp13-30,2007.

[5] Wankar, Priyanka, Sharma, Anand, Sinhal,Ruchika "Performance Analysis and Implementation Perfect Difference Network Using NS2".IJLTET,Vol2, Issue 1, 2013

[6] Tiwari,S.,Katare,R.K." A Study of Hex-cell, complete graph and Perfect Difference Network (PDN), 2nd International Confrence on Emerging Trends in computer science,communication and information Technology,ISBN978-81-923487-1-1(2015).

[7] Tiwari sunil, Katare R.K.," A Study of Fabric of Architecture Using Structural Pattern and Relation",Internatioal journal of latest technology in engeneering, management and applied science,ISSN No.2278-2540,p-33-37,vol IV Issue IX Sep.2015.

[8] Rakov, M. And J. Machall , "Method of Interconnection Functional Nodes and a Hyperstar I [Rako98] Rakov, M., "Method Of Interconnecting Nodes and a Hyperstar Interconnection Structure ," US Patent 5 734 580, issued March 1998.

[9] Parhami B. and Rakov M.A., "Perfect Difference Networks and Related Interconnection Structures for Parallel and Distributed Systems," IEEE Transactions on Parallel and Distributed Systems , Vol. 16, No. 8 , August 2005.

[10] Tiwari S.,Katare R.K., "Alliance Study of Perfect Difference Network & Hex-Cell Architecture**".** International Journal of Emerging Technology and Advanced Engineering,volume 5,Issue 3,march 2015 p-25.

[11] Katare Rakesh, Tiwari Sunil, "Hamiltonian, Topological properties of Hex-Cell and Perfect Difference Network (PDN) for design new Hybrid Architecture for Parallel System,**"**National Seminar on Recent Trends in Science and Technology",March 30-31, 2015 , MPCST,Bhopal(M.P.)

[12] P. Guerrier and A. Grenier, "A Generic Architecture for on Chip Packetswitched Interconnections," In Proc. Design Automation and Test in Europe Conf. (DATE), pp. 250-256,2000.

[13] Patrikar Rajendra and Gaikwad M., "Perfect Difference Network for Network Chip Architecture," International Journal of C.S., Vol.9, Dec. 2009.

[14] www.wikipedia.com

[15] Hwang Kai, " Advanced Computer Architecture: Parallelism, Scalability, Programmability. ", McGraw-Hill Book Co. International Edition, 1993.

[16] Parhami, B., Fellow, IEEE, and Rakov, M., Performance, Algorithmic, and Robustness Attributes of Perfect Difference Networks, IEEE transactions on parallel and distributed systems, vol. 16, no. 8, August 2005.

[17] Wu, Xingfu and Sun, Xian-He, "Performance Modeling for Interconnection Networks", IEEE, 2000.

[18] [KUMAR04] A. Kumar, S. Tiwari, "Defect Tolerance for Nanocomputer Architecture", International Workshop on System-Level Interconnect Prediction, Paris, France February 14-15 2004, 89-96.

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